Universidade de São Paulo - São Carlos,SP
Instituto de Ciências Matemáticas e de Computação

USP - ICMC - SSC
SSC 0610 - Eng. Comp. - 2o. Semestre 2010

Disciplina de Organização de Computadores I

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Material on-line Wiki ICMC - http://wiki.icmc.usp.br/index.php/Ssc-610

Aula 02s

Apresentação da Disciplina

Agenda:

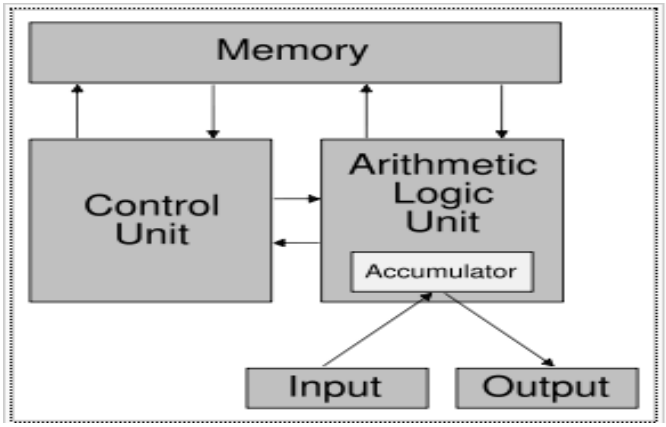
1. **Arquitetura de Von Neumann:**
   ULA, Memória, Registradores, UC e E/S
2. **Memória – Conceitos Básicos**

- **Flip-Flops, Registradores e Contadores**
- **Registradores: Acumulador**
- **Registradores: Registro de Instrução**
- **Registradores: Contador de Programa**
- **Registradores: Flags**
- **Memória: Barramento e Acesso a Memória**

1. Arquitetura de Von Neumann

Arquitetura - Modelo Inicial:

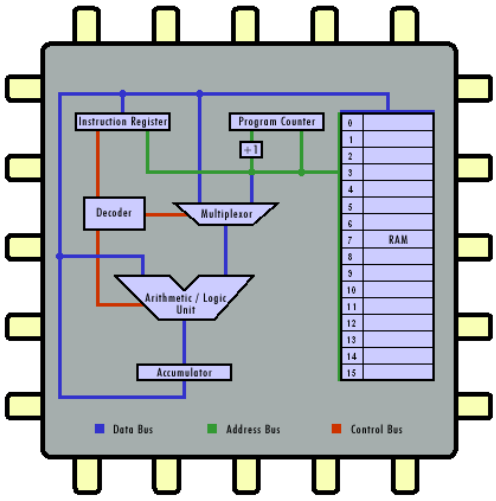
- Máquina de von Neumann



Refs: http://en.wikipedia.org/wiki/Von_Neumann_architecture

1. Arquitetura de Von Neumann

CPU – Processador

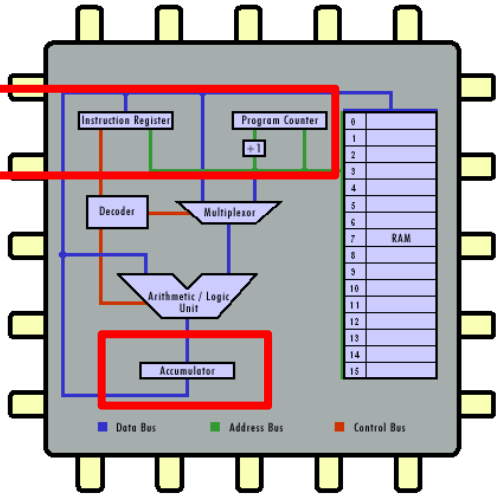


Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

1. Arquitetura de Von Neumann

CPU – Processador

Registradores



Registradores

Program Counter: PC (CP)
Instruction Register: IR (RI)
Accumulator: Acc (AC)
Status Register - Flags: Flags

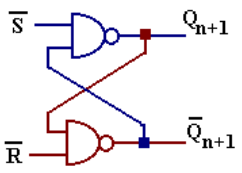
Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Conceitos Básicos

FLIP-FLOP RS Básico

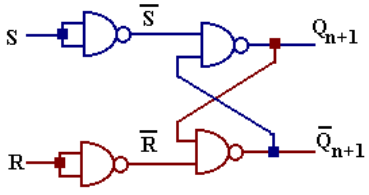
Memória de 1 bit

FLIP-FLOP RS



$\overline{S}$	$\overline{R}$	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	proibida		
0	1	1	0	Estado Set
1	0	0	1	Estado Reset
1	1	Q_n	$\overline{Q}_n$	Latch (memória)

FLIP-FLOP RS



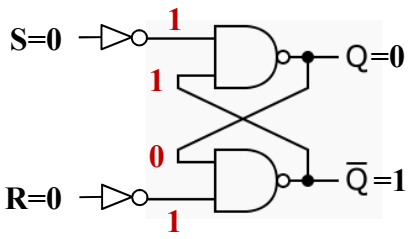
S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	Q_n	$\overline{Q}_n$	Latch (memória)
0	1	0	1	Estado Reset
1	0	1	0	Estado Set
1	1	proibida		

Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Conceitos Básicos

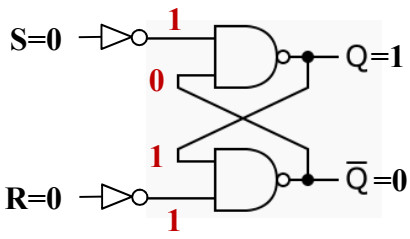
FLIP-FLOP RS Básico

Memória de 1 bit



$Q_{(t-1)} = 0$

$\overline{Q}_{(t-1)} = 1$



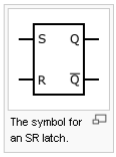
$Q_{(t-1)} = 1$

$\overline{Q}_{(t-1)} = 0$

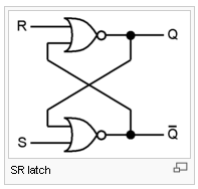
2. Memória – Conceitos Básicos

SR LATCH (FLIP-FLOP)

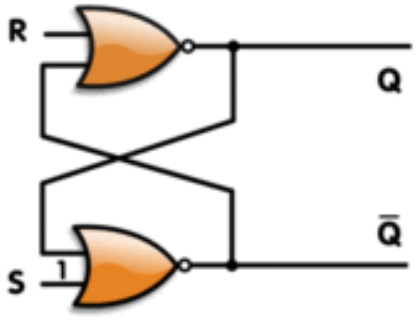
SR latch operation		
S	R	Action
0	0	Keep state
0	1	Q = 0
1	0	Q = 1
1	1	Restricted combination



The symbol for an SR latch.



SR latch

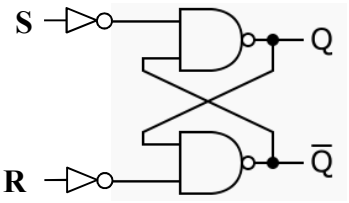


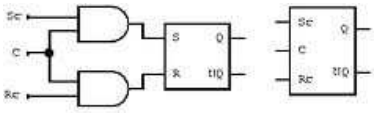
Memória de 1 bit

2. Memória – Conceitos Básicos

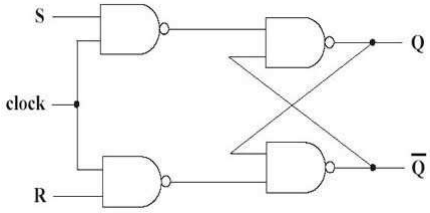
FLIP-FLOP RS com Clock

Memória de 1 bit





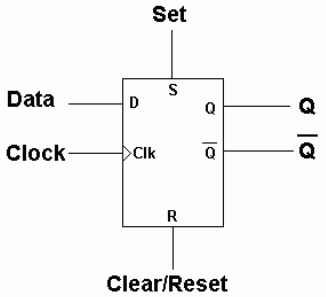
S_C	R_C	C	Q	$\overline{Q}$
x	x	0	no change	
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	undefined	
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	undefined	



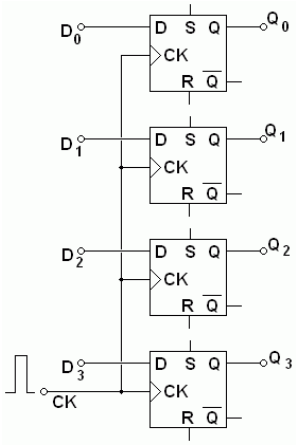
Flip-Flop:
RS, RS + Clock,
D, JK, Master-Slave

2. Memória – Conceitos Básicos

D LATCH (FLIP-FLOP)



Memória de 1 bits

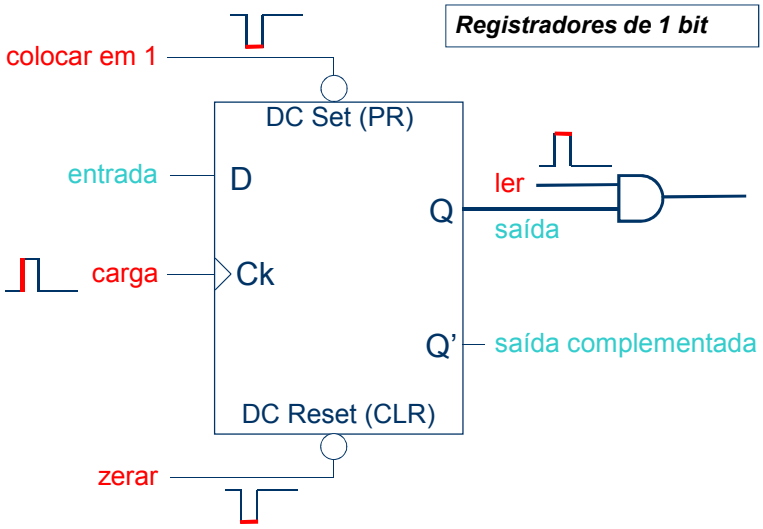


Memória de 4 bits

2. Memória – Conceitos Básicos

Unidade de Memória

Registradores de 1 bit



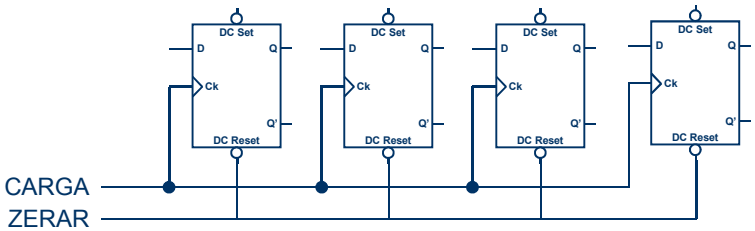
Fonte: ftp://ftp.inf.ufrgs.br/pub/inf107/ (RegMemAlu)

2. Memória – Registradores

Unidade de Memória

Registradores de de vários bits

- um flip-flop por bit
- sinais de controle comuns a todos os flip-flops

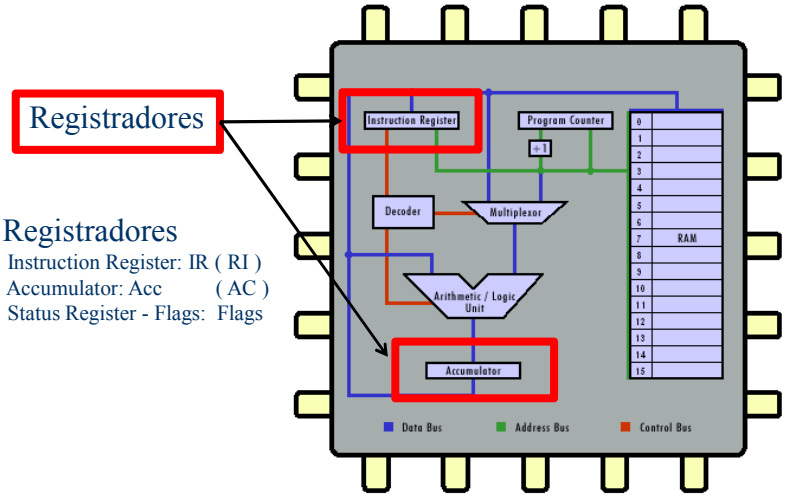


Quando lê as entradas ?
- nas bordas positivas do sinal **CARGA**

Quando zera todos os bits ?
- quando o sinal **ZERAR** passa de 1 para 0

2. Memória – Registradores

CPU – Processador



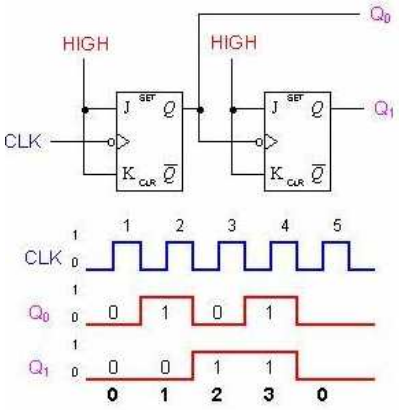
Registradores
Instruction Register: IR (RI)
Accumulator: Acc (AC)
Status Register - Flags: Flags

Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Registradores

Registrador - Contadores

- JK master-slave sensíveis à borda de **descida**

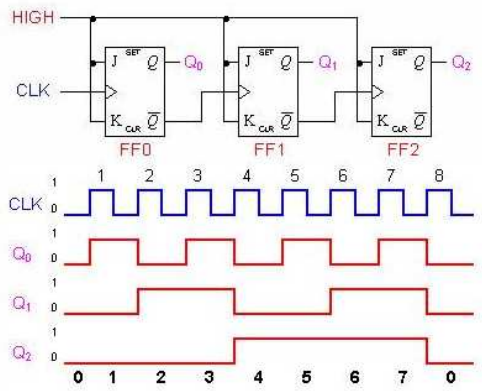


Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Registradores

Registrador - Contadores

flip-flops JK master-slave sensíveis à borda de **subida** do controle CLOCK



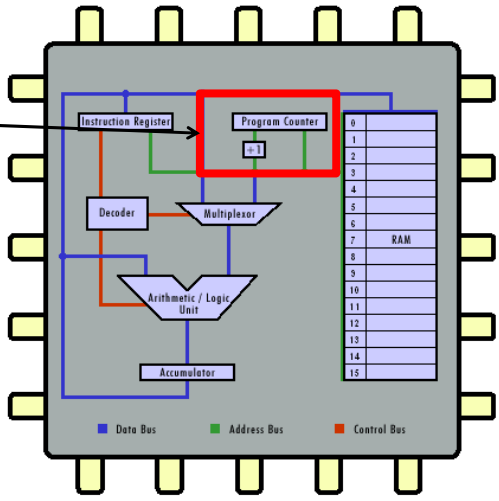
Fonte: http://endigital.orgfree.com/sequencial/sequencial.htm

2. Memória – Registradores

CPU – Processador

Registradores

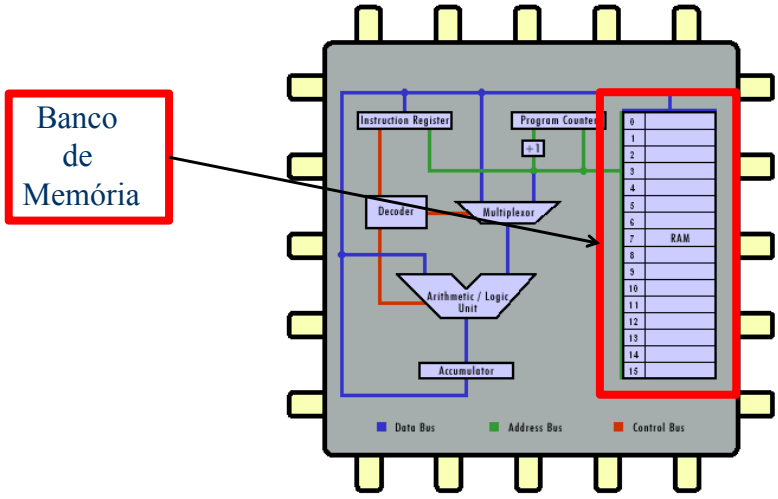
Registradores
Program Counter: PC



Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

2. Memória – Registradores

CPU – Processador

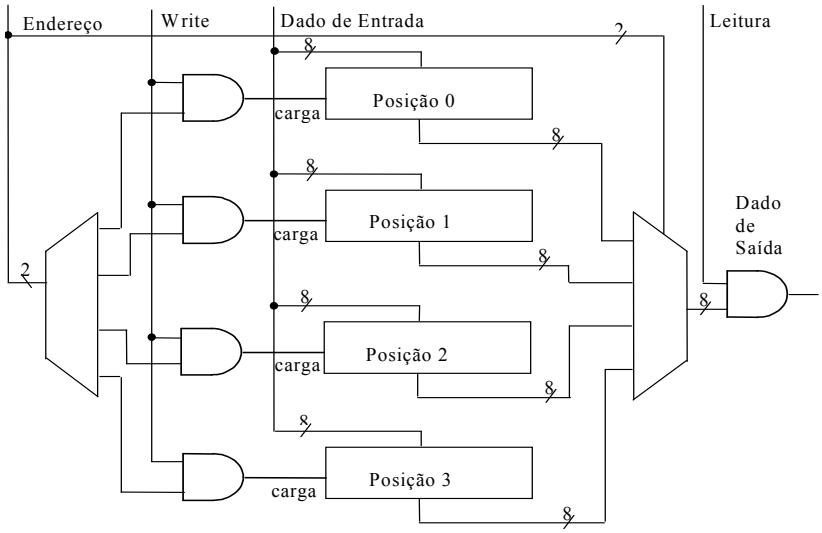


Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

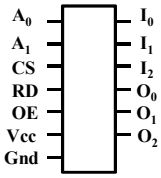
2. Memória – Banco de Memória

Unidade de Memória

Memória com seleção linear

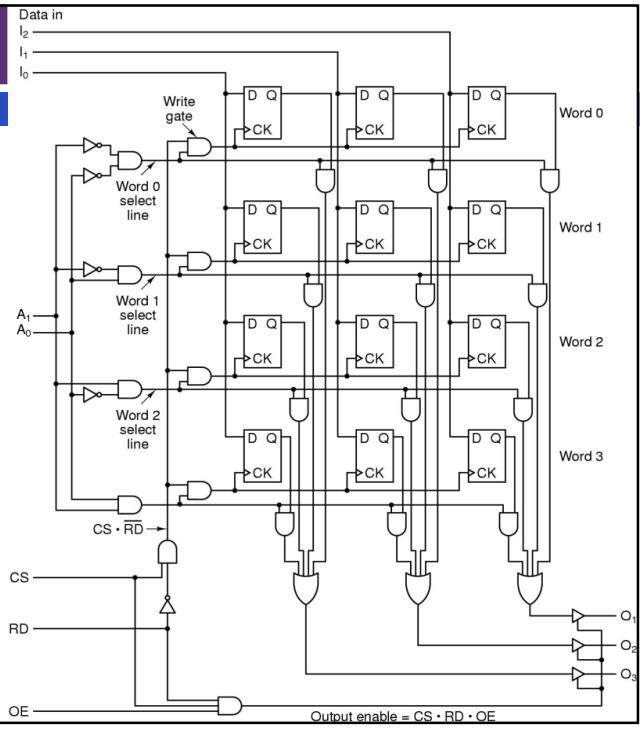


Memória



Memória 4 x 3:
4 Endereços de
3 bits cada

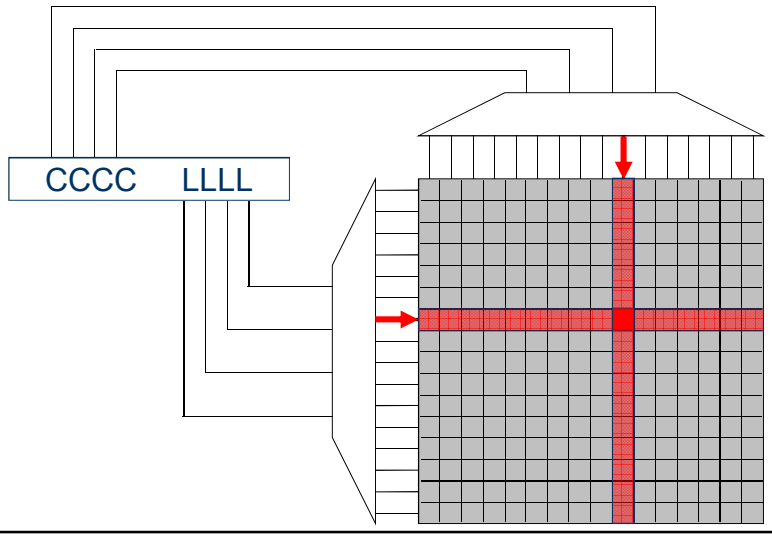
Endereços: A_0 .. A_1
Dados (in): I_0 .. I_2
Dados (out): O_0 .. O_2
CS = Chip Select
RD = Read
OE = Output Enable



2. Memória – Banco de Memória

Unidade de Memória

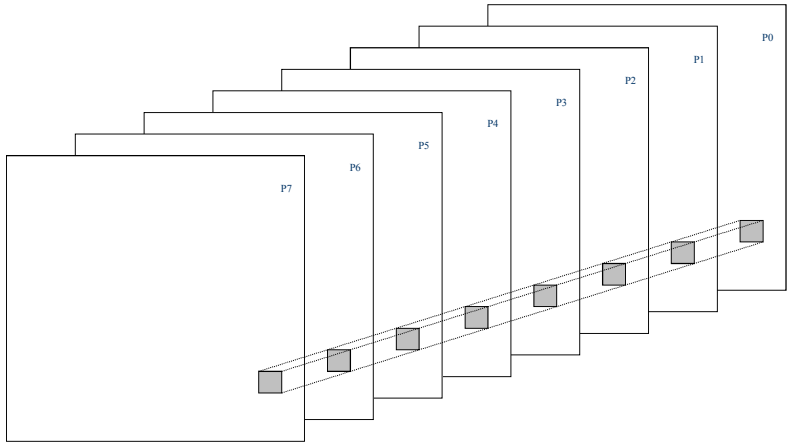
Memória com seleção matricial (um "plano")



2. Memória – Banco de Memória

Unidade de Memória

Memória com seleção de plano
(1 bit em cada "plano")

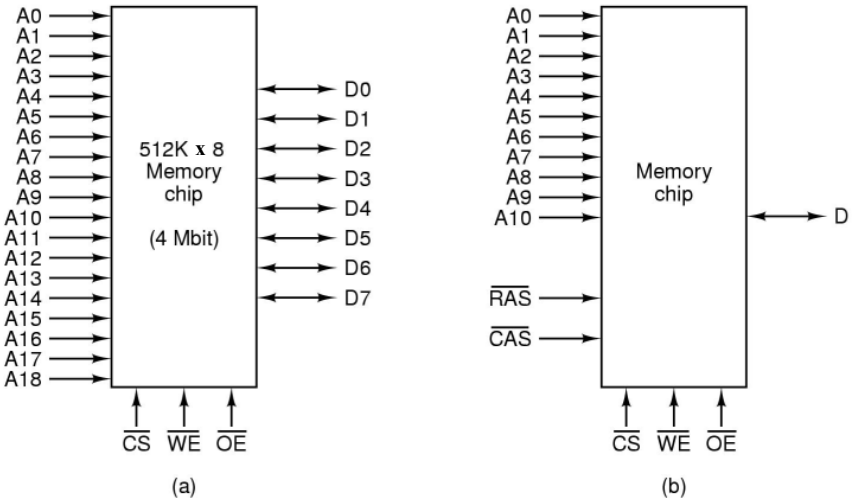


(1 "plano" pode ser 1 circuito integrado de memória "*n*k × 1 bit")

2. Memória – Banco de Memória

Unidade de Memória

Static and Dymanic RAM

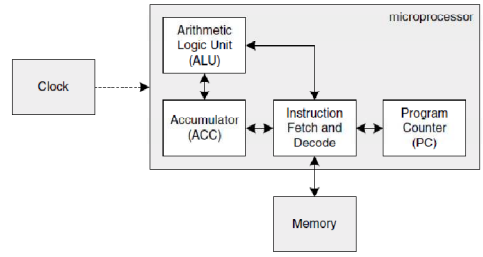


Fonte: http://www.carlosfelgueiras.hpg.com.br/Cursos/ArqComp/aula_5.html

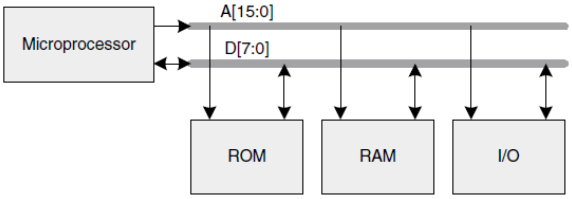
2. Memória, Registradores e E/S

Arquitetura de Computadores

Fonte: Mark Balch - Complete Digital Design



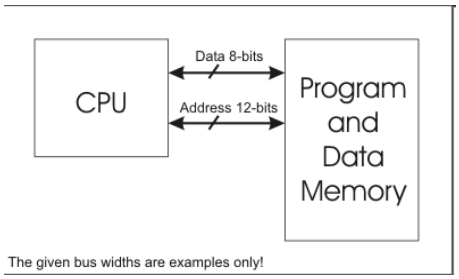
Simple microprocessor



Microprocessor buses

2. Arquitetura de Von Neumann

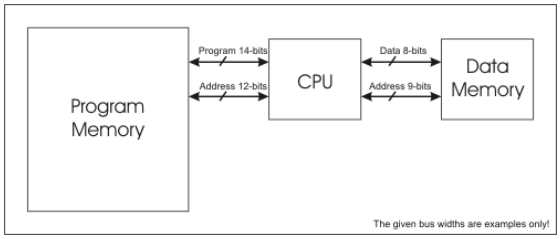
Arquitetura: *Von Neumann x Harvard*



Máquina de Von Neumann

Instruções:
Operador + Operando

IAS
8 bits - Operação (OPcode)
12 bits - Operando (Endereço)



Arquitetura de Harvard

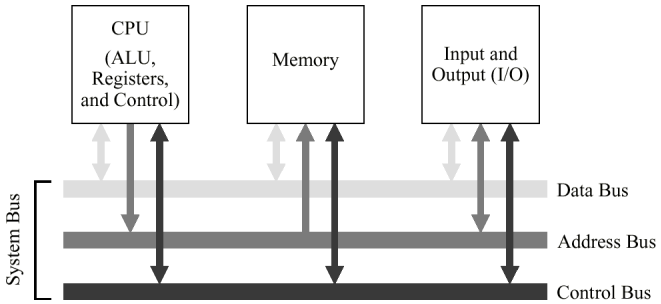
- Separação entre memória de programa e memória de dados
- Busca de instruções e operandos pode ser simultânea (barramentos separados)

Fonte: http://www.elec.canterbury.ac.nz/PublicArea/Staff/hof/p10-embed/p10-tutorial/p13.html

2. Arquitetura de Von Neumann

Arquitetura de Computadores:

Barramentos: Endereços, Dados e Controle

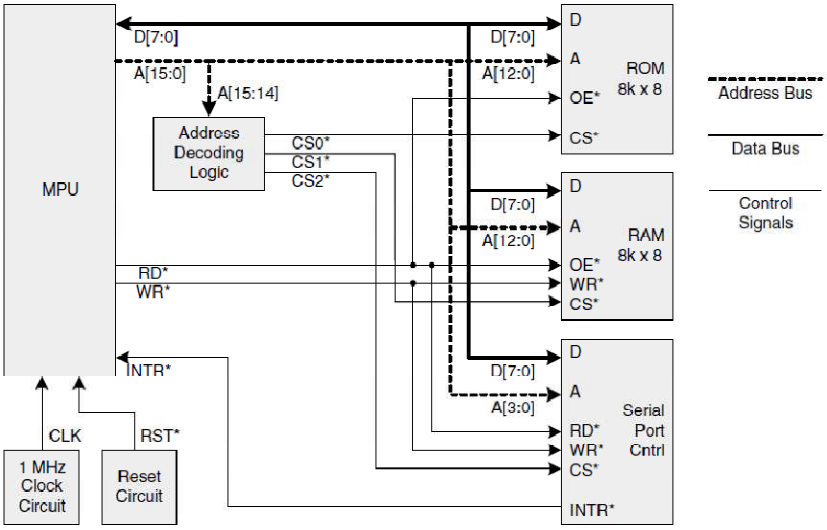


Fonte: http://williamstallings.com/COA6e.html

2. Arquitetura de Von Neumann

Arquitetura de Computadores

Eight-bit computer block diagram



2. Arquitetura de Von Neumann

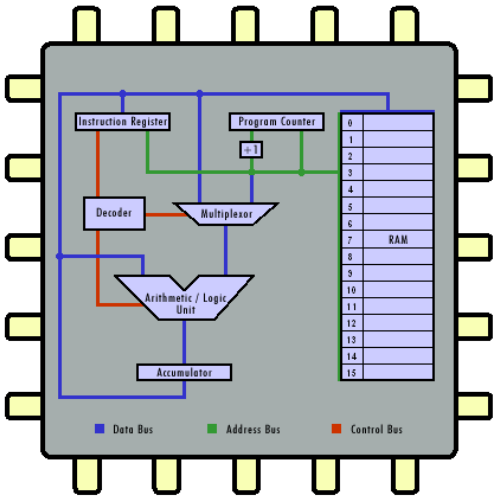
Unidade de Controle - UC

- Responsável por gerar todos os sinais que controlam as operações no exterior do CPU, e ainda por dar todas as instruções para o correto funcionamento interno do CPU [UC é o "Maestro da Orquestra"];
- Junto a Unidade de Controle temos um decodificador de instruções, que analisa e decodifica o Operador da Instrução (OPcode);
- A unidade de controle executa três ações básicas intrínsecas e pré-programadas pelo próprio fabricante do processador, são elas:
  - (i) busca (fetch)
  - (ii) decodificação
  - (iii) execução
- Assim sendo, todo processador, ao iniciar sua operação, realiza uma operação cíclica, tendo como base essas três ações. A unidade de controle usualmente é fixa, onde esta define o Conjunto de Instruções do Processador: CPU *Instruction Set*

2. Arquitetura de Von Neumann

Unidade de Controle - UC

Show time...



Fonte: http://courses.cs.vt.edu/~csonline/MachineArchitecture/Lessons/CPU/index.html

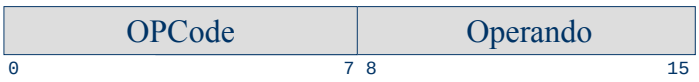
2. Arquitetura de Von Neumann

Unidade de Controle - UC

CPU Instruction Set

Código de Instruções

Operador da Instrução + Operando(s)



Exemplo: Instrução de 16 Bits

Tipos de Instruções...
Arquiteturas de 4, 3, 2, 1 e 0 endereços

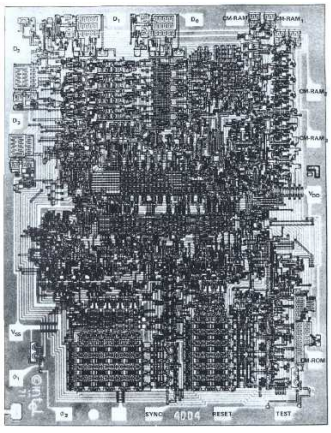
Tipos de Instruções... Conjunto de Instruções Microprogramado
Tipos de Instruções... RISC, CISC, VLIW
Tipos de Instruções... Modo de Endereçamento
Tipos de Instruções... Instruções de Controle, Privilegiadas, etc.

Fonte: ftp://ftp.inf.ufrgs.br/pub/inf107/ (Arquiteturas de 0,1,2,3,4 endereços)

3. Arquitetura de Microprocessadores - Intel 4004

Intel 4004 (1971)

16-pin DIP package
P-channel Silicon Gate MOS
Minimum system: CPU and one ROM
4-bit parallel CPU with 45 instructions



MCS-4
FOUR-BIT PARALLEL MICROCOMPUTER SET

Features

- Microprogrammable General Purpose Computer Set
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- Addition of Two 8-Digit Numbers in 850 Microseconds
- 2-Phase Dynamic Operation
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-4 ROMs and RAMs
- Easy Expansion — One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Unlimited Number of Output Lines
- Packaged in 16-Pin Dual In-Line Configuration
- Directly Compatible With 4004 CPU
- Interface 1702A PROMs Directly to 4004 CPU -- Completely Eliminates TTL Interface
- Permits Program Storage in Alterable Memory
- Execute MCS-4 Programs from any Mix of Standard Intel PROMs, ROMs and RAMs
- Expanded I/O Port Capability
- Each Port May be Both Input and Output -- Up to 16 4-bit Input Ports and 16 4-bit Output Ports
- I/O Ports and Control Lines are TTL Compatible
- Number of I/O Ports is Independent of the Size of the Program Memory
- New Instruction WPM (Write Program Memory) is Used for Loading Alterable Program Storage (RAM)

3. Arquitetura de Microprocessadores - Intel 4004

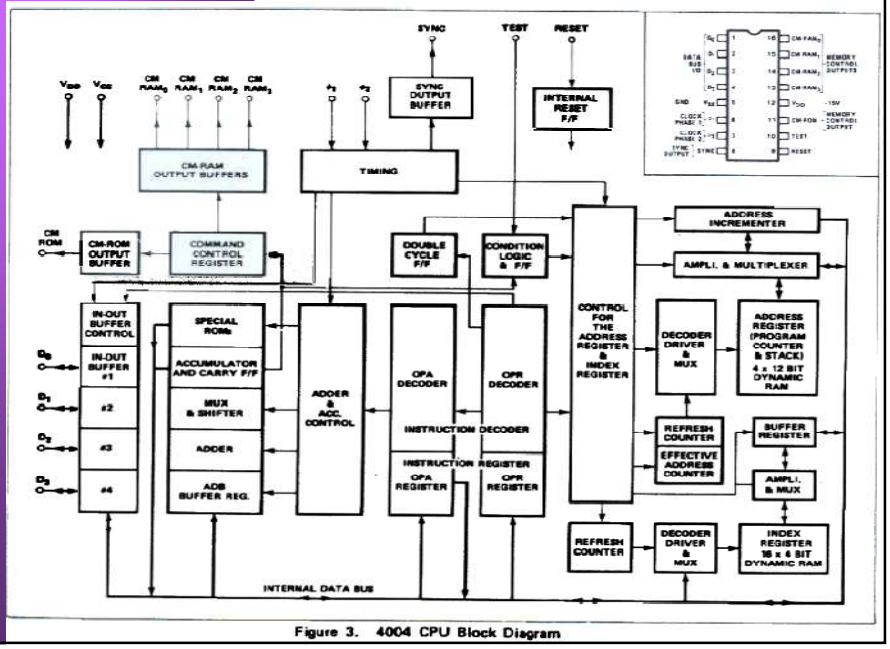
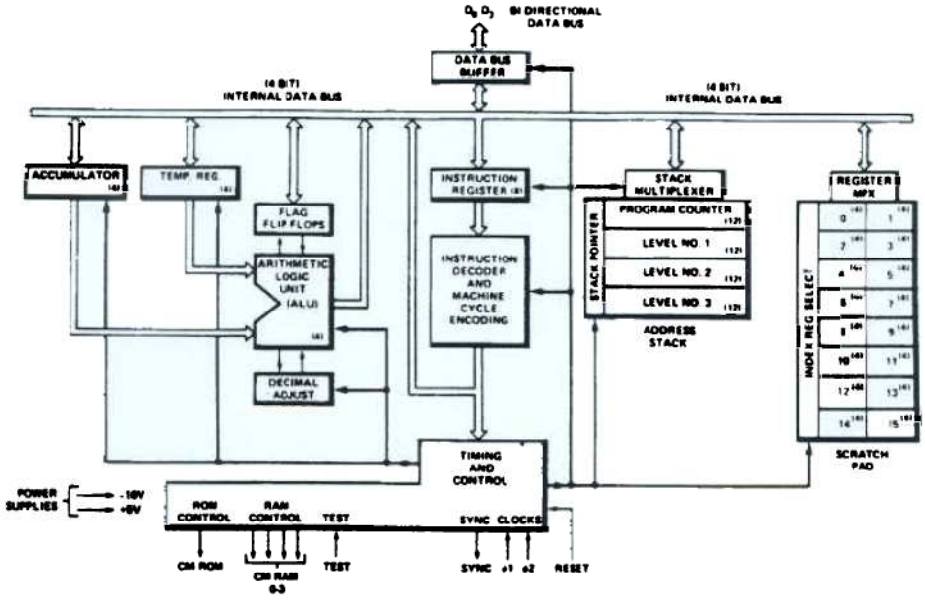


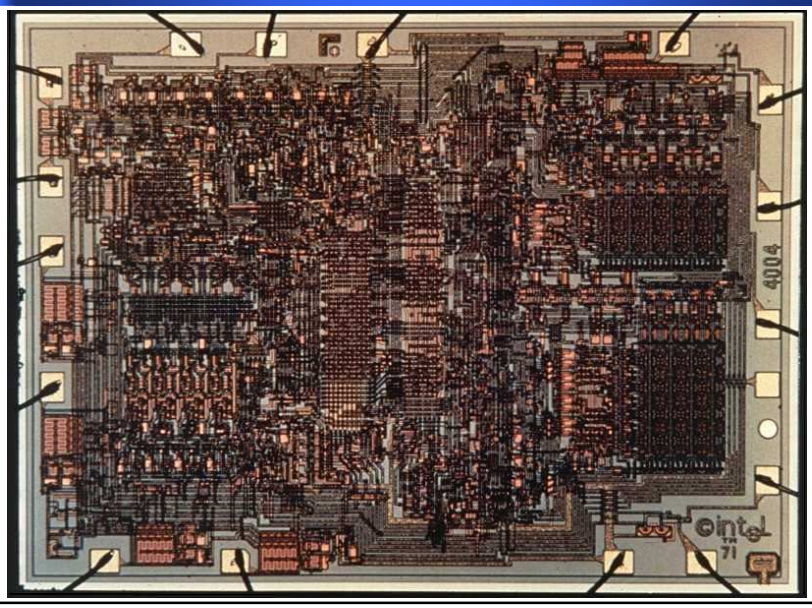
Figure 3. 4004 CPU Block Diagram

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3. Arquitetura de Microprocessadores - Intel 4004



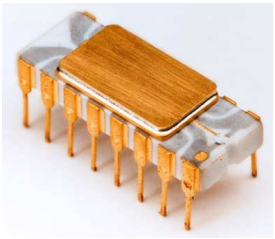
3. Arquitetura de Microprocessadores - Intel 4004

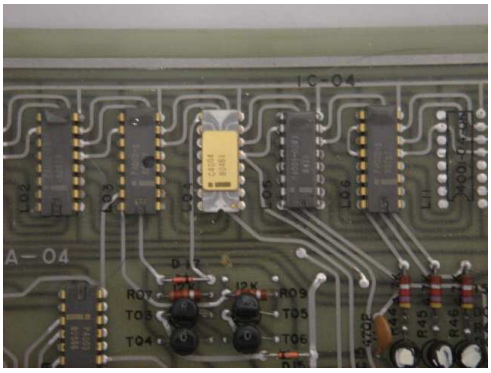


3. Arquitetura de Microprocessadores - Intel 4004

Intel 4004

Busicom - Nippon Calculating Machine Corp changed its name to Business Computer Corporation, was a Japanese company that owned the rights to the first microprocessor but sold them back to Intel. They made electronic calculators and the first using the new Intel 4004 processor was the Busicom 141-PF[1]









INFORMAÇÕES SOBRE A DISCIPLINA

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